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Comparative Analysis of Power Dissipation for CMOS Inverter & Adiabatic Logic Inverters

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Abstract—*The power dissipation of CMOS inverter with other adiabatic inverters is reported in this paper. The simulation of all the circuits are done using Tanner EDA tool at 180nm technology. With the simulation results power dissipation of CMOS inverter and adiabatic inverters namely PFAL, ECRL, PAL, 2N2N2P are confirmed. The comparative study of all these inverters has shown that PFAL adiabatic inverter has least power dissipation among all.*

1. INTRODUCTION

In today's scenario the dependability on electronic gadgets is increasing. Small size, low power consumption and portability are the prime concern. For any electronic device, inverter is the basic requirement. There are various techniques for designing of inverters like conventional CMOS inverter logic, adiabatic inverter logics etc.

The different standard logics styles which have been used before are used to implement inverter and these inverters are compared with each other in this paper. Though their operation is same but they have different transistor count and also different functioning at the intermediate nodes. Each logic style has its own advantages and disadvantages like if some logic gives high speed of operation then it may be at the cost of high power consumption. Basically the PAT i.e. power, area and time determines the performance of any device.

This paper has considered some of the performance criterion for designing and evaluation of various inverter designs. This paper has four sections. Section I describes the introduction. Section II gives the literature review of different inverter logics. Section III comprises of simulation results which are then compared. Section IV concludes the work.

2. LITERATURE REVIEW

2.1 Conventional Complementary MOSFET Inverter

The Fig. is showing the circuit of CMOS inverter. In this, the nMOS and pMOS are in complementary mode. The pMOS network is known as Pull-Up network and the nMOS network is known as Pull-Down network. When the input is high the nMOS drives the output i.e. pull- down and when the input is low the pMOS drives the output i.e. pull up. It has small power dissipation due to leakage current but for steady state, the power dissipation is virtually negligible.

The supply voltage is Vdd and C is the capacitance so during pull up the charge delivered to the load is $Q=CVdd$. The total energy supplied by the supply is $E = QVdd$ or $E = CVdd^2$. The capacitor stores energy in the form of charge so the total energy stored by the capacitor is $E_{charge} = ½\ CVdd^2$. While during pull down the capacitor is discharged through ground and the same amount of energy is dissipated in discharging [1].

Total Energy is $E = CVdd^2$

$E = E_{charge} + E_{discharge}$

$E = ½\ CVdd^2 + ½\ CVdd^2 = CVdd^2$

During charging and discharging operation half of the total energy is wasted in the form of heat.

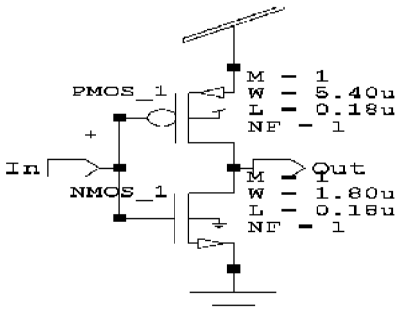

Fig. 1: Conventional CMOS inverter

2.2 Adiabatic inverters

Adiabatic circuits work on the principle of reusing or recycling the energy drawn from power supply. In these circuits the load capacitance is charged by a constant current source (as shown in figure2) which corresponds to linear voltage ramp. The non-standard time varying voltage supplies are required in these circuits. The energy dissipation in adiabatic circuits can be calculated by $E = (RC/T).CV^2$.

For adiabatic circuits, the charging time should be more than 2RC to have less power dissipation than conventional CMOS. The reduction in on-resistance of PMOS network reduces the power dissipation. The charge stored in capacitor is transferred back to supply in order to reuse the power [1].

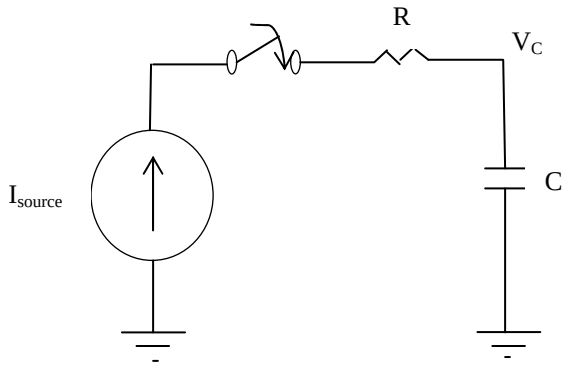

Fig. 2: Load capacitance *C* charging by a constant current source through resistance *R*.

2.2 1 Efficient charge recovery logic adiabatic inverter (ECRL)

This adiabatic inverter has two cross coupled PMOS and similar structure as of Cascade Voltage Switch Logic (CVSL). The latch used in this is made by two PMOS only. To efficiently recover the charge delivered four phase clocking rule is used by ECRL [2].

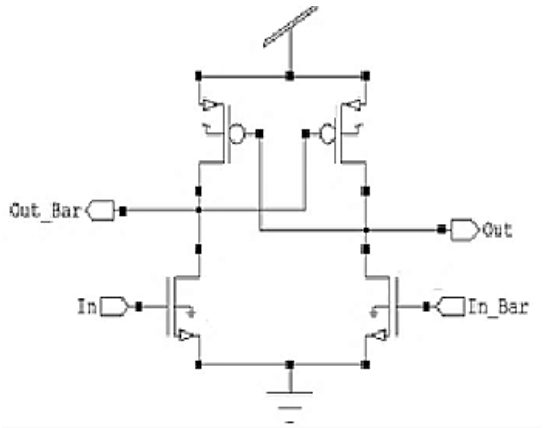

Fig. 3: ECRL adiabatic inverter.

2.2 2 Positive feedback adiabatic logic inverter (PFAL)

Among the similar logic families it consumes lowest power and it is more robust than other. Using two NMOS and two PMOS a latch is made which is the core of all PFAL circuits. In parallel, the functional blocks are added with transmission PMOS. This helps in maintaining resistance small for the charging of capacitor [2-3].

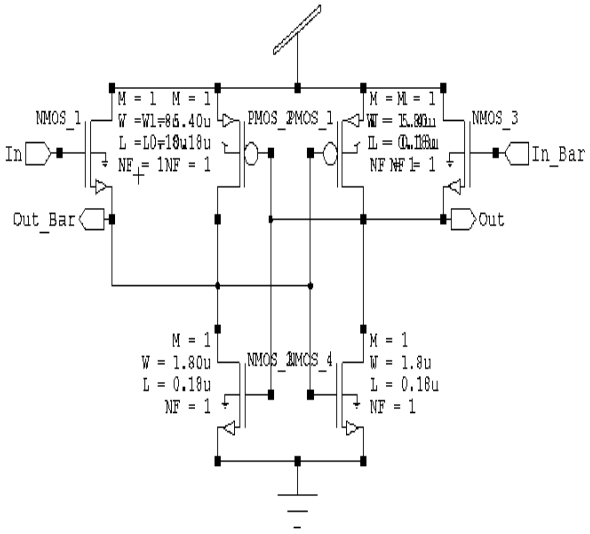

Fig. 4: PFAL adiabatic inverter.

2.2.3 Pass transistor adiabatic logic inverter (PAL)

It is relatively a less gate complex dual rail adiabatic inverter which operates with two phase power clock. It also has cross coupled PMOS latch as of ECRL adiabatic inverter. Energy saving and switching noise characteristics improvements are exhibited by PAL family [4].

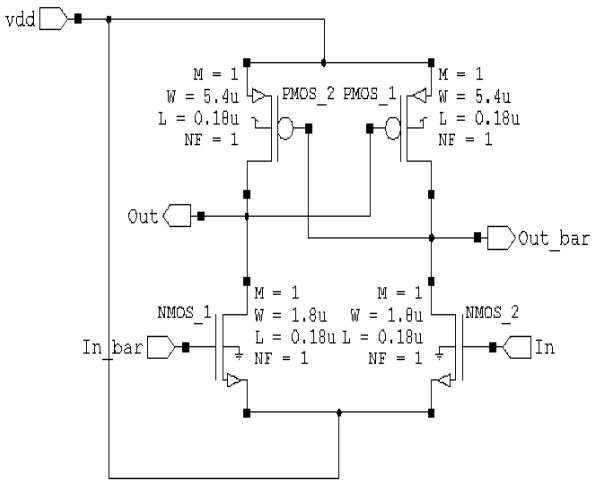

Fig. 5: PAL adiabatic inverter

2.2.4 2n2n2p adiabatic logic inverter

To reduce the coupling effect 2N2N2P family was derived from 2N2P. In this, the latch is made by two PMOS and two NMOS while in 2N2P latch is made by two PMOS only [3].

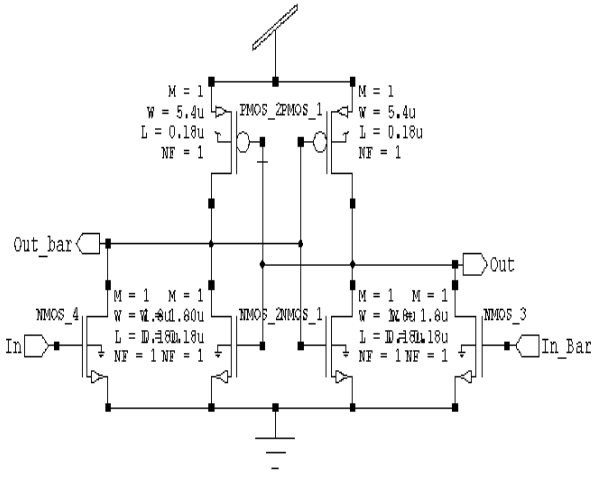

Fig. 6: 2N2N2P adiabatic inverter.

3. SIMULATION RESULTS

The simulation is done at 180nm technology for comparison of power dissipation. The circuits are designed in Tanner EDA tool and simulated at normal room temperature. The maximum supply voltage used is 1.8V. From the simulation results it has been observed that PFAL adiabatic inverter has the lowest power dissipation.

3.1 Output waveforms of inverters

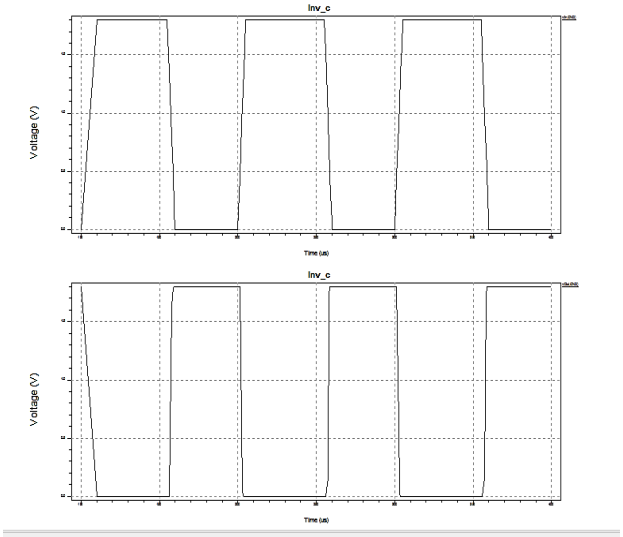

Fig. 7. CMOS inverter output waveform.

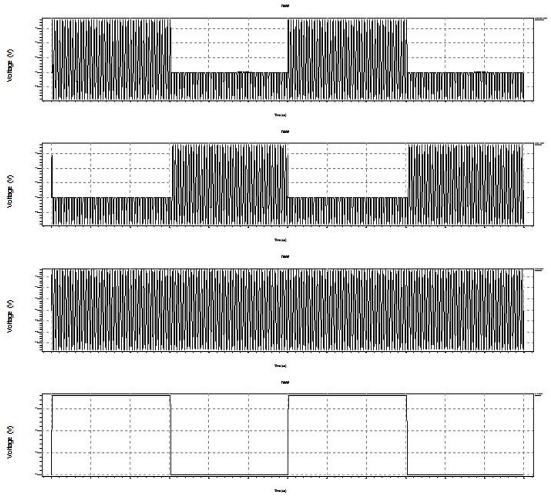

Fig. 8: ECRL adiabatic inverter.

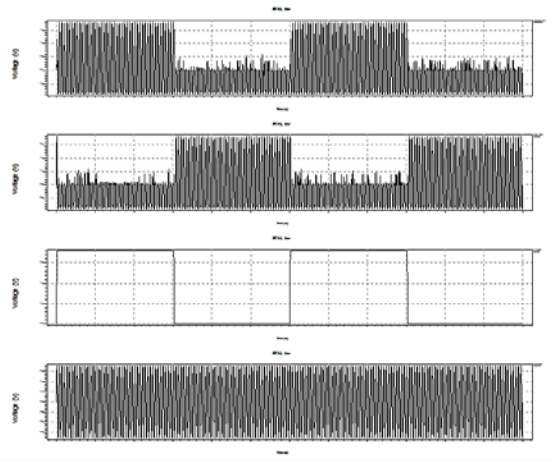

Fig. 9: PFAL adiabatic inverter.

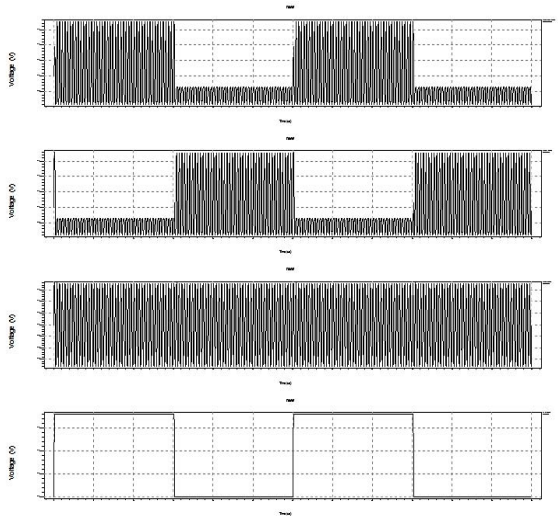

Fig. 10: PAL adiabatic inverter.

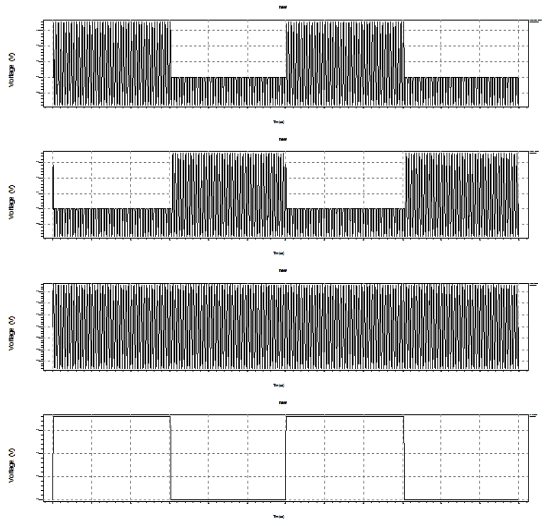

Fig. 11: 2N2N2P adiabatic inverter.

3.2 Power Comparison of Inverters

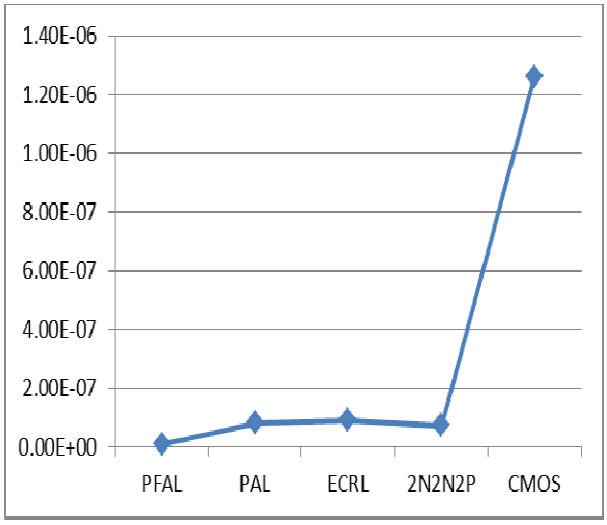

Fig. 13: Power dissipation of different inverters.

Y-axis is denoting the power dissipation and X-axis is denoting the inverters.

4. CONCLUSION

This paper is a comparative study of different inverter logics. Conventional CMOS, ECRL, PFAL, PAL and 2N2N2P adiabatic inverters are first implemented and then their SPICE simulation is done. The power dissipation of these circuits is compared and it has been found that CMOS has the more power dissipation than adiabatic inverters and among all inverters PFAL has the lowest power dissipation.

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